ERROR DETECTING ARITHMETIC CIRCUITS USING HEXADECIMAL DIGITAL ROOTS

ABSTRACT OF THE DISCLOSURE

Embodiments of the invention are directed to circuits and techniques for computer processor register integrity checking employing digital roots, and hexadecimal digital roots (HDRs) in particular, to validate the results of arithmetic operations and register moves. These circuits thus provide extra confidence that register operations were correctly executed. A hexadecimal digital root is computed for the result of each register computation and compared to the results of the same computation performed on the HDRs of the operands. The hexadecimal digital root approach may be simply implemented with standard combinatoric logic. Validation is accomplished in a single clock cycle so that there is no added system delay or latency. The circuits and methods described herein have comparatively little impact on processor real estate.